

ABSTRACT OF THE DISCLOSURE

Each wiring layer of a multilayered wiring substrate (100) comprises signal wirings (31a to 31n) disposed in parallel with one another, and dummy wirings (31Da, 31Dn) disposed at each side of the signal wiring group (31) made by signal wirings (31b to 31m), respectively. The dummy wirings (31Da, 31Dn) have the same shape as the signal wirings (31a to 31n), and are disposed in parallel to the signal wirings (31b to 31m) at the same intervals as that in the signal wirings (31a to 31n). Through holes (40ab to 40mn) are formed in the respective clearances among the signal wirings (31a to 31n). Dummy through holes (40Da, 40Dn) having the same shape as the through holes (40ab to 40mn) are formed between the dummy wiring (31Da, 31Dn) and signal wiring (31a, 31n). A conductive layer is formed on the inner wall of the through holes (40ab to 40mn, 40Da, 40Dn). With the multilayered wiring substrate (100), it is able to reduce or eliminate the delay time difference between signals that propagate along the signal wirings.